IN THE CLAIMS

Please amend the claims as follows:

1. (Previously Presented): A chip on chip (COC) device comprising:

a logic chip having a logic circuit;

a memory chip mounted on the logic chip, the memory chip comprising: basic chips functioning as a chip independently from each other; and a dicing line interposed between the basic chips, connecting the basic chips, and configuring a part of the memory chip;

a bump connecting the logic chip and the memory chip; and

at least one of an alignment mark and a test element group provided in the dicing line, wherein the basic chips have a bump.

2. (Original): The COC device according to claim 1, wherein the basic chips have all the same layout.

3. (Previously Presented): The COC device according to claim l, wherein at least a first portion of the basic chips has a layout that is inverted with respect to a layout of a second portion of the basic chips.

4. (Canceled).

5. (Original): The COC device according to claim 1, wherein in the case where the basic chips are square, one side of individual basic chips has a length of 2 mm or more.

6. (Original): The COC device according to claim 5, wherein the dicing line has a width of 0.1 mm.

7. (Canceled).

8. (Original): The COC device according to claim 1, wherein the basic chips have a circuit capable of changing a word organization by a control signal.

9. (Currently Amended): A chip on chip (COC) device comprising:

a logic chip having a logic circuit;

a memory chip mounted on the logic chip, the memory chip comprising: basic chips functioning as a chip independently from each other, and changing a specification of each basic chip by a control signal; and a dicing line interposed between the basic chips, connecting the basic chips, and configuring a part of the memory chip; and

a bump connecting the logic chip and the memory chip;

wherein the control signal is supplied from the logic chip to the memory chip and the basic chips have a bump.

10. (Original): The COC device according to claim 9, wherein the basic chips have all the same layout.

11. (Previously Presented): The COC device according to claim 9, wherein at least a first portion of the basic chips has a layout that is inverted with respect to a layout of a second portion of the basic chips.

12. (Previously Presented): The COC device according to claim 9, further comprising at least one of an alignment mark and a test element group provided in the dicing line.

13. (Previously Presented): The COC device according to claim 9, wherein in a case where the basic chips are square, one side of individual basic chips has a length of 2 mm or more.

14. (Original): The COC device according to claim 13, wherein the dicing line has a width of 0.1 mm.

15. (Canceled).

16. (Previously Presented): A system in package device comprising:

the COC device according to claim 1; and

a package covering said COC device.

17. (Previously Presented): A system in package device comprising:

the COC device according to claim 9; and

a package covering said COC device.

18. (Previously Presented): The COC device according to claim 9, wherein the specification is a word organization of the basic chip.

19. (Previously Presented): The COC device according to claim 9, further comprising a flash memory chip mounted on the logic chip, wherein the memory chip having the basic chips is a DRAM chip.

20. (Previously Presented): The COC device according to claim 9, further comprising a DRAM chip mounted on the logic chip, wherein the memory chip having the basic chips is a flash memory chip.